REMARKS

By this amendment, Applicants have amended the title to be more clearly indicative of the invention to which the claims are directed, as required by the Examiner. Applicants have also amended claims 9 and 13 to eliminate the informalities noted by the Examiner.

In view of the foregoing amendments to claims 9 and 13, reconsideration and withdrawal of the objections to these claims are requested.

Claims 1, 2, 4-9 and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,255,706 to Watanabe et al. in view of U.S. Patent No. 6,678,017 to Shimomaki et al. Applicants traverse this rejection and request reconsideration thereof.

The present invention relates to a display device having thin film transistors on a substrate. The display device includes gate patterns, in each of which a gate line and a gate electrode of a thin film transistor are integrally formed, and drain lines. The gate pattern is constituted by at least three-layered films consisting of a lowermost layer, an intermediate layer formed of at least one layer and an uppermost layer at least at either a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line. The intermediate layer is formed of a material selected from the group consisting of pure Al, and Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy, and the uppermost layer and the lowermost layer are formed of a metal having a melting point higher than the melting point of the material of the intermediate layer. As set forth in independent claim 1, end portions of the intermediate layer are recessed from end portions of the uppermost layer and end

portions of the lowermost layer. As set forth in independent claim 7, end portions of the uppermost layer of the gate electrode are spaced inwardly from end portions of the lowermost layer and, at the same time, end portions of the intermediate layer of the gate electrode are recessed from end portions of the uppermost layer and end portions of the lowermost layer.

The patent to Watanabe et al. discloses a thin film transistor wherein at least one of (1) a gate electrode and/or a scanning line therefor and (2) source/drain electrode and/or signal lines therefor comprises a laminated wiring structure in which a main wiring layer formed of a metal selected from Al, Cu or an alloy based on the metal is sandwiched between an underlying wiring layer and an overlaying wiring layer. The underlining and overlying wiring layers are formed of a material based on a metal or alloy of metals and containing nitrogen, the metal being selected from Ti, Mo, W, Cr, Al, Cu, and the materials used in the underlying and overlaying wiring layers being different from each other. As admitted by the Examiner, the Watanabe et al. patent does not disclose end portions of an intermediate layer recessed from end portions of an uppermost layer and an end portions of a lowermost layer, as presently claimed.

The Examiner refers to Figure 10B of Shimomaki et al. and alleges this patent to disclose a display device having a three-layer gate pattern where end portions of an uppermost layer (104a) of the gate electrode are spaced inwardly from end portions of the lowermost layer (102) and, at the same time, end portions of the intermediate layer (103) are recessed from end portions of the uppermost layer and end portions of the lowermost layer. However, Figure 10B of Shimomaki et al.

shows an intermediate stage of the manufacturing process. That is, Figure 10B shows only an early formation step before the data line is completed. The completed data line is shown in Figure 10E and clearly does not have the structure of the presently claimed gate pattern. Accordingly, there is no suggestion in Shimomaki et al. that an intermediate structure at an early formation step should be used in a completed device. To the contrary, the Shimomaki et al. patent suggests that a different structure (the structure of Figure 10E) be used in the completed device. Accordingly, there is no motivation to use the structure from the formation step shown in Figure 10B of Shimomaki et al. in the completed structure of Watanabe et al. Therefore, the combined teachings of Watanabe et al. and Shimomaki et al. would not have suggested the presently claimed invention.

For the foregoing reasons, the presently claimed invention is patentable over the proposed combination of Watanabe et al. and Shimomaki et al.

Claims 3 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. in view of Shimomaki et al. and further in view of U.S. Patent No. 6,018,308 to Jeong et al. Applicants traverse this rejection and request reconsideration thereof.

The patent to Jeong et al. relates to a method for manufacturing liquid crystal displays and discloses the use of a Mo, Mo, W layer as a wiring by itself of large scale and high resolution liquid crystals. However, clearly nothing in Jeong et al. remedies the basic deficiencies noted above with respect to Watanabe et al. and Shimomaki et al. Accordingly, claims 3 and 10 are patentable over the proposed combination of references.

Claim 13 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. in view of Shimomaki et al. and further in view of patent application publication number U.S. 2001/0005020 A1 to Jinno et al. Applicants traverse this rejection and request reconsideration thereof.

The Jinno et al. publication discloses a thin film transistor which can be used in an LCD display panel. The Examiner has cited the Jinno et al. publication as showing a TFT for a display in which LDD regions are formed on a semiconductor layer and overlap portions of the gate electrode to increase the OFF resistance of the TFT. However, clearly nothing in Jinno et al. remedies the basic deficiencies noted above with respect to the combination of Watanabe et al. and Shimomaki et al. Therefore, claim 13 is patentable over the proposed combination of references.

Applicants note the indication of allowable subject matter in claims 11 and 12. However, in view of the foregoing amendment and remarks, it is submitted all of the claims now in the application are in condition for allowance.

Applicants note the Examiner has cited a number of documents as being pertinent to applicants' disclosure. However, since these documents has been applied in rejecting the claims formerly in the application, further discussion of these documents is deemed unnecessary.

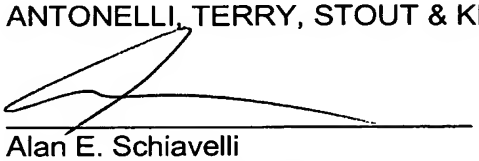
In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing

of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.43456X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Alan E. Schiavelli
Registration No. 32,087

AES/at
(703) 312-6600